

Ben Le

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PROFESSIONAL SUMMARY

Computer Engineering graduate student with hands-on experience in embedded systems, real-time firmware development, and FPGA-based hardware design. Background spans FreeRTOS, CAN bus integration, FPGA synthesis workflows, and low-level hardware bring-up including lab bench verification (oscilloscopes & multimeters), soldering, and circuit design. Published researcher with experience leading lab teams and presenting technical work at national conferences.

EDUCATION

University of California, Irvine (UCI)

M.S. in Electrical & Computer Engineering, Concentration in Computer Engineering.

Irvine, CA

Expected Jun 2028

California State University, Fullerton (CSUF)

B.S. in Computer Engineering, Minor in Aging Science. Scholarships: CSUF Alumni

Fullerton, CA

May 2026

Association Student Scholarship, OLLI Aging Science Award. GPA: 3.98/4.0.

Relevant Coursework: Signals & Systems, RTOS, Cyberphysical Security, Intro to GPS, Computer Design & Organization

EXPERIENCE

Undergraduate Lab Head

Aug 2024 – May 2026

Brain-Computer Interface Lab, CSUF

Fullerton, CA

- Engineered a low-latency UDP bridge between Python and MATLAB Simulink modules to synchronize memory tasks with neural recordings, achieving less than 20ms synchronization latency
- Published paper, "Band Power Associations of Memory in Older Adults using Electroencephalography," at IEMCON 2025, and presented posters at 4 research conferences
- Provided guidance for graduate thesis projects, including a realtime robotic arm control loop using CSP filtering and an LSTM model, and an artifact filtering method for resting-state tasks

VHDL Instructional Student Assistant

Aug 2024 – Aug 2025

Engineering and Computer Science Department, CSUF

Fullerton, CA

- Mentored 90+ students in digital logic design, debugging ModelSim/Vivado workflows and verifying structural/behavioral VHDL implementations, contributing to a 90%+ class passing rate
- Taught K-maps, testbench creation, static timing analysis, and encoder/decoder implementations
- Proctored exams and supported students on behalf of professors during laboratory hours

Undergraduate Research Assistant

May 2023 – Aug 2023

ASSURE-US Program

Remote

- Benchmarked power and area efficiency of 4 lightweight ciphers on Artix-7 FPGA hardware, running synthesis/implementation workflows to record Slice LUTs, Registers, and Bonded IOBs
- Presented findings as posters at NCUR 2024 and SCCUR 2023 conferences

PROJECTS

Quadconn

May 2025 – May 2026

Senior Design

- Interfaced with BLDC motor controllers using FD-CAN, sending angular positions and receiving diagnostic data at 200 Hz across 12 BLDC motors concurrently, split across 3 CAN buses to meet robotic stance timing constraints
- Integrated Iceoryx2 inter-process communication to connect control and publisher/subscriber nodes
- Implemented audiovisual data collection using GStreamer, transmitting data via UDP packets through a Tailscale tunnel to enable low-latency long-distance communication

TENS Game Unit

Aug 2025 – Dec 2025

Personal Project

- Used FreeRTOS to program an ESP32 as a bridge between a TENS unit and a PC, using tasks to manage open-drain GPIO connections and UART communication
- Developed a threshold-based computer vision model using OpenCV to detect a video game character's downed state and send commands to the ESP32 bridge
- Identified PCB switches using a multimeter, soldered wired connections to enable communication between the ESP32 and the TENS unit, and verified connectivity using oscilloscope measurements

SKILLS

Languages: C, C++, VHDL, Verilog, Python, MATLAB

Tools & Frameworks: FreeRTOS, Xilinx Vivado, ModelSim, KiCAD, Docker, Linux, Git